REMARKS

This paper is responsive to the Final Office action dated May 25, 2006. Claims 1-44 were examined. Claims 1, 10, 13, 24 were rejected, claims 2-9, 11-12, 14-23, 25-35 were indicated as being allowable if rewritten in independent form, and claims 37-44 were allowed.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 10, 13, and 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hikawa et al. (U.S. Patent No. 5,666,304). Applicant respectfully traverses this rejection.

Regarding claim 1, the Examiner has indicated that Hikawa discloses, *inter alia*, a three-dimensional memory array, citing column 21, lines 13-30 in support thereof. The cited passage states:

> The sense circuit 36 detects ranges to which the ON-state current values of the memory cells M0 to M3 belong, and converts the same to the *three-dimensional data {(A), (B), (C)}* as shown in FIG. 7. In more concrete terms, {(A), (B), (C)} are {"H", "H", "H"} for the type 0 memory cell M0, {"L", "H", "H"} for the type 1 memory cell M1, {"L", "L", "H"} for the type 2 memory cell M2, and {"L", "L", "L"} for the type 3 memory cell M3. The data {(A), (B), (C)} are transmitted to the decision circuit 37. The decision circuit 37 converts the three-dimensional data {(A), (B), (C)} received from the sense circuit 36 to 2-bit data ((1), (2)). In more concrete terms, ((1), (2))=(H, H) when {(A), (B), (C)}={"H", "H", "H"}, i.e., when the type 0 memory cell M0 is selected, ((1), (2))=(H, L) when {(A), (B), (C)}={"L", "H", "H"}, i.e., when the type 1 memory cell M1 is selected, ((1), (2))=(L, H) when {(A), (B), (C)}={"L", "L", "H"}, i.e., when the type 2 memory cell M2 is selected, and ((1), (2))=(L, L) when {(A), (B), (C)}={"L", "L", "L"}, i.e., when the type 3 memory cell M3 is selected.

(Column 21, lines 11-30). Applicant respectfully suggests that the discussion of the "three-dimensional data {(A), (B), (C)}" has been mis-interpreted by the Examiner. Rather, Hikawa's "three-dimensional data {(A), (B), (C)}" relates to storing *multiple bits per memory cell*, and is disclosed only in the context of *two-dimensional* memory arrays. Hikawa nowhere describes an integrated circuit having a three-dimensional memory array (i.e., two or more memory planes).

A somewhat more extensive reading of Hikawa reveals the accuracy of Applicant's assertion. Fig. 4 clearly shows that the three-dimensional data (A), (B), and (C) are generated by

a sense amplifier 36 is response to a single memory cell, which could be of type M0, M1, M2, or M3. For example, Hikawa states:

> As shown in FIG. 4, each of the bit lines 25 and 26 is connected to an external sense circuit 36 through a bit line selecting transistor 35. While a sense circuit is generally employed for reading ROM data, the sense circuit 36 is absolutely identical to a well-known one in a point that the same detects values of currents flowing in the memory cells M0 to M3. Namely, the sense circuit 36 is adapted to detect the range to which an ON-state current value of *a selected memory cell* belongs, for converting the same to *three-dimensional data {(A), (B), (C)}*. This sense circuit 36 has threshold voltages which can decide three types of current values, i.e., those which are set between (0) and (i), between (i) and (ii), and between (ii) and (iii) in FIG. 6 respectively.

(Column 19, lines 12-24). Further, this three-dimensional data is converted into 2-bit data by the decision circuit 37 shown in Fig. 4, according to the chart depicted in Fig. 7, as Hikawa describes:

> As shown in FIG. 4, the sense circuit 36 is connected to a decision circuit 37 through 3-bit output lines corresponding to the three-dimensional data {(A), (B), (C)} respectively. As shown in FIG. 7, the decision circuit 37 has functions of deciding which one of the type 0 to 3 memory cells M0 to M3 is selected on the basis of the three-dimensional data {(A), (B), (C)} received from the sense circuit 36 and converting the three-dimensional data {(A), (B), (C)} to 2-bit data ((1), (2)).

(Column 19, lines 31-40). The passage cited by the Examiner essentially describes this same behavior. Lastly, Hikawa summarizes a major goal of this arrangement by stating:

> Thus, each of the memory cells M0 to M3 has multivalue characteristics as 2-bit data ((1), (2)), whereby the number of memory cell transistors provided in the memory cell array can be halved as compared with the prior art in which a single memory cell transistor corresponds to 1-bit data, and the area of the memory cell array portion can also be halved. In other words, it is possible to double the storage capacity in the same area as that in the prior art. Thus, it is possible to improve the degree of data integration by remarkably reducing the chip size of the ROM at about the same degree of refinement as the prior art, thereby enabling cost reduction and implementation of mass storage. In more concrete terms, a 32-megabit ROM can be formed by about 16 mega memory cells according to the present invention, while about 32 mega memory cells are required in the prior art.

(Column 21, lines 31-45). The three-dimensional data {(A), (B), (C)} are nothing more than a respective signal (described in Fig. 7) conveyed on each of three nodes (described in Fig. 4), all responsive to a single selected memory cell. Hikawa does not disclose all the limitations of claim 1, and therefore cannot be viewed as anticipating this claim.

Regarding claim 10, the Examiner again indicated that Hikawa discloses a three-dimensional memory array, citing the same passage in support thereof. Again this rejection must fall, for the same reasons given above.

Regarding claim 13, the Examiner indicated that Hikawa discloses a three-dimensional memory array having at least two planes of memory cells formed above a substrate, citing Fig. 25, M0-M3 on substrate 71, and Column 25, lines 25-27. Applicant respectfully submits that this passage, likewise, does not disclose this limitation. This passage is introduced in regards to Fig. 25-27. Fig. 25 is described as being a plan view (i.e., "top" view), and even a cursory review of Fig. 26 will show that only a single layer of transistors is formed on the substrate 71, and can only represent a single memory plane. There is not even a scintilla of suggestion in any of the figures of a three-dimensional memory array, as used and claimed by Applicant. Therefore, Hikawa does not disclose all the limitations of claim 13, and cannot be viewed as anticipating this claim.

Regarding claim 24, this claim is believed allowable at least for its dependence from an allowable claim 13.

Hikawa does not disclose all the limitations of the rejected claims. Consequently, Applicant respectfully submits the rejection is improper and requests the rejection be withdrawn.

Claims 1, 10, and 13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kaske et al. (U.S. Patent No. 3,696,349). Applicant respectfully traverses this rejection.

Regarding claim 1, the Examiner has indicated that Kaske discloses, *inter alia*, an integrated circuit having respective decode/selection circuits respectively located along opposite edges of a three-dimensional memory array. The Examiner generally cites Fig. 11, and the text at column 9, lines 25-26, lines 30-31, and lines 43-46 in support of this assertion. Applicant

respectfully submits that Kaske does not disclose an integrated circuit at all. Moreover, Kaske does not even disclose decode/selection circuits on opposite sides of his array.

As to the memory array, Kaske describes:

> A three-dimensional magnetizable memory *stack* of Mated-Film memory elements each of which provides a substantially closed flux path, except for a gap transverse to the element's easy axis, is disclosed. *The stack is comprised of a plurality of superposed, i.e., laid one upon the other so as to make all like-oriented-parts vertically coincide,* similar transfer arrays sandwiched between a write array and a read array, all arrays having similarly arranged Mated-Film write/read, transfer memory elements with a gap in the top layer for providing an external longitudinal steering field $\pm H_L$ across the gap that is inductively coupled to each next superposed memory element.

(Abstract, lines 1-13). Kaske states that the "two-dimensional write/read array 8 consists of a substrate member 10 upon which are deposited parallel sets of bit/sense lines 12..." (Column 3, lines 48-50). Continuing, Kaske states the "two-dimensional transfer array 28 consists of a substrate member 30 upon which are deposited parallel word or transfer lines 32a, 32b, 32c, 32d." (Column 4, lines 3-6). Kaske clearly describes a memory array fashioned by physically stacking a plurality of individual structures, each formed upon its own substrate. Such a structure is not an integrated circuit.

Regarding the assertion that Kaske discloses decode/selection circuits on opposite sides of his array, the Examiner has stated that one such pair of oppositely disposed decode/selection circuits shown in Fig. 11 includes labeled elements 222 and 226, and another such pair of oppositely disposed decode/selection circuits shown in Fig. 11 includes labeled elements 220 and 224.

Applicant respectfully submits that the elements 224 and 226 are not decode circuits, but are described merely as being "terminals", while the element 220 is described as being a "word driver 220," and the element 222 is described as being a "$\pm H_L$ bit driver 222." Similarly, all the other labeled structures above 224 are likewise described as being mere "terminals". In particular, Kaske writes:

> With particular reference to FIG. 11 there is presented a diagrammatic illustration of a memory system incorporating the three-dimensional memory stack of the present invention. Memory system 200 includes a three-dimensional memory stack 202 that is comprised of a bottom write array 204, superposed transfer arrays 206, 208, 210, 212, 214, 216 and superposed top read array 218. These two-dimensional arrays of Mated-Film write, transfer and read (memory) elements are illustrated as conforming to the arrangements of FIGS. 1 and 2; however, many other arrangements may be possible such as write/read arrays containing a plurality of separate word lines whereby a plurality of separate multibit words may be selectively written into the write array and individually and selectively passed through the three-dimensional memory stack as required. Coupled to write array 204 are; H_T *word driver 220*, $\pm H_L$ *bit driver 222*, *terminal 224* and *terminal 226*; coupled to read array 218 are, H_T word driver 230, gated sense amplifier 232, *terminal* 234 and *terminal* 236; coupled to transfer arrays 206, 208, 210, 212, 214, 216 are H_T word drivers 240, 242, 244, 246, 248, 250, respectively, and *terminals* 300, 302, 304, 306, 308, 310, respectively.

(Column 8, line 62 through column 9, line 19). Nowhere does Kaske ever again mention these terminals. But whatever there are, and whatever they do, they cannot be viewed as being a word driver, such as word drivers 220, 240, 242, 244, 246, 248, 250, and 230. Even assuming, *arguendo*, that such a word driver may be viewed as a decode/selection circuit, Kaske does not disclose decode/selection circuits on *opposite* sides of his array, either for the bit lines or for the word lines. In fact, there is no other bit driver described other than the $\pm H_L$ bit driver 222, as element 232 is described as being a sense amplifier 232.

Applicant respectfully submits that the claim clearly recites a structure which is not taught or suggested by Kaske, and requests that the rejection be withdrawn as to this claim.

Regarding the rejection of claim 10, the Examiner relies upon the same argument as for claim 1. Applicant likewise submits that Kaske does not disclose or suggest the claimed structure, and requests that the rejection be withdrawn as to this claim.

Regarding the rejection of claim 13, the Examiner again cites Fig. 11 to support his argument, this time citing element 220 and 222 as having outputs associated with word lines or bit lines which exit on opposite edges of the array. Clearly such elements are not disposed on opposite sides of the array, but even assuming that the Examiner meant to cite elements 220 and 224, or to cite elements 222 and 226, the argument fails, for elements 224 and 226 are clearly disclosed as *not* being decode or selection circuits, nor even *driver* circuits, but merely *terminals*.

Again, Applicant submits that Kaske does not disclose or suggest the claim structure, and requests that the rejection be withdrawn as to all three rejected claims.

Allowable Subject Matter

Claims 2-9, 11-12, 14-23, 25-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In light of the believed allowability of the independent claims, these claims remain without amendment.

Claims 37-44 are allowed.

Summary

Claims 1-44 remain in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Should any issues remain, Applicant respectfully requests a telephonic interview with the Examiner to discuss this response, and further in the hope that the remaining issues might be efficiently resolved.

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Andrew C. Graham — Date: 8-25-06

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